UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,904	10/12/2005 John R. Cutter		GB030046US1	4540
65913 NXP, B.V.	7590 01/29/200	EXAMINER		
· ·	ECTUAL PROPERTY	SITTON, NELSON		
1109 MCKAY	DRIVE	ART UNIT	PAPER NUMBER	
SAN JOSE, CA	x 95131	4158		
			NOTIFICATION DATE	DELIVERY MODE
			01/29/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

		Annlies	tion No	Annlicent(a)				
		Арріїса	Dilication No. Applicant(s)					
		10/552	,904	CUTTER ET AL.				
Office Action Summary			ıer	Art Unit				
		NELSO	N SITTON	4158				
Period fo	The MAILING DATE of this communic	cation appears on t	he cover sheet wit	th the correspondence ac	ddress			
	• •	D DEDLY 10 OFT	TO EVEIDE - M	ONITH ((0) OR THURTY (0	20. 54.40			
WHIC - Exte after - If NC - Failu Any	ORTENED STATUTORY PERIOD FO CHEVER IS LONGER, FROM THE MAnsions of time may be available under the provisions of SIX (6) MONTHS from the mailing date of this commu operiod for reply is specified above, the maximum state re to reply within the set or extended period for reply we reply received by the Office later than three months afted patent term adjustment. See 37 CFR 1.704(b).	ALING DATE OF far the	THIS COMMUNIC event, however, may a red will expire SIX (6) MON' application to become AB.	CATION. eply be timely filed THS from the mailing date of this of the control o	·			
Status								
1) 又	Responsive to communication(s) filed	Lon 12 October 20	205					
2a)□	Responsive to communication(s) filed on <u>12 October 2005</u> . This action is FINAL . 2b) This action is non-final.							
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is							
٥/ك	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
	·	o unao. En parto (gaay,0, 1000 0.D.	, , , , , , , , , , , , , , , ,				
Disposit	ion of Claims							
4)🛛	Claim(s) <u>1-15</u> is/are pending in the application.							
	4a) Of the above claim(s) is/are withdrawn from consideration.							
5)□	Claim(s) is/are allowed.							
6)⊠	Claim(s) <u>1-15</u> is/are rejected.							
7)🛛	Claim(s) <u>8</u> is/are objected to.							
8)□	Claim(s) are subject to restrict	ion and/or electior	ı requirement.					
Applicat	ion Papers							
9) ☐ The specification is objected to by the Examiner.								
, —	•		cepted or b)🛛 ol	bjected to by the Examir	ner.			
,—	10)☑ The drawing(s) filed on <u>12 October 2005</u> is/are: a)☐ accepted or b)☑ objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
	Replacement drawing sheet(s) including t		-	• •	FR 1.121(d).			
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
Priority (ınder 35 U.S.C. § 119							
		or foreign priority (ınder 35 H.S.C. &	119(a)-(d) or (f)				
	12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)⊠ All b)□ Some * c)⊠ None of:							
	1.⊠ Certified copies of the priority documents have been received.							
	 2. ☐ Certified copies of the priority documents have been received. 2. ☐ Certified copies of the priority documents have been received in Application No 							
	3. Copies of the certified copies of the priority documents have been received in this National Stage							
	application from the International Bureau (PCT Rule 17.2(a)).							
* 5	* See the attached detailed Office action for a list of the certified copies not received.							
Coo and alaboriou dotailou chied dotain for a list of the doftinou doplos not received.								
Attachmen	t(s)							
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)								
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date Notice of Informal Patent Application								
B) ☑ Information Disclosure Statement(s) (PTO/SB/08) Statement(s) (PTO/SB/08) Faper No(s)/Mail Date 10/12/2005. 5) ☑ Notice of Informal Patent Application 6) ☐ Other:								
,	. ,		· - -					

Art Unit: 4158

DETAILED ACTION

1. Claims 1-15 are presented for examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawing 1 is objected to because reference character 50, which has been used to designate "control inputs" in the description, is not shown on the drawing 1. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

Art Unit: 4158

pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
- (e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
- (f) BACKGROUND OF THE INVENTION.
 - (1) Field of the Invention.
 - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (g) BRIEF SUMMARY OF THE INVENTION.
- (h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
- (i) DETAILED DESCRIPTION OF THE INVENTION.
- (j) CLAIM OR CLAIMS (commencing on a separate sheet).
- (k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).

Appropriate correction is required.

Art Unit: 4158

9-10).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claim 8 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in the reply filed on 10/12/2005. In that paper, applicant has stated that "a freewheel mode in which the energise FET is off and both the control and freewheel FETs are off", and this statement indicates that the invention is different from what is defined in the claim(s) because according to the specification, the control FET may be switched on and the energise FET 4 switched off to give a freewheel mode (page 9, line

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 8. Claims 10, 11 and 12 are rejected under 35 U.S.C 102(b) as being anticipated by Gu (US Pub No. 2004/0160725 A1 hereinafter).
- 9. As to claim 10, Gu discloses a driver, comprising:

Art Unit: 4158

a battery terminal and a ground terminal for connection to a voltage battery output and a ground battery output, respectively (24, GND, fig. 1);

an output terminal for driving a coil (22, fig. 1);

high and low side driver FETs integrated in a common substrate and connected between the battery terminal and the output terminal and the ground terminal and the output terminal, respectively (26, 28, 30, fig.1);

high-side control circuitry capable of operation when the voltage on the common substrate is at least 1V above the voltage on the ground terminal integrated in the common semiconductor substrate, the high-side control circuitry being connected to the gates of the high side driver FET or FETs to control the high side driver FET or FETs (26, 28, fig.1; paragraph 0023, lines 1-11); and

low-side control circuitry capable of operation even when the voltage on the common substrate is close to the voltage on the ground terminal integrated in the common semiconductor substrate, the low-side control circuitry being connected to the gates of the low side driver FET or FETs to control the low side driver FET or FETs (26, 30, fig.1; paragraph 0025, lines 1-11);

- 10. As to claim 11, Gu discloses a driver where the FETs are each n-type (28, 30, fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ other types of switching devices, such as for example, p-type FETs.
- 11. As to claim 12, Gu discloses a coil control circuit, comprising:

Art Unit: 4158

a driver (fig. 1);

a battery having a voltage battery output connected to the battery terminal of the driver and a ground battery output connected to the ground terminal of the driver (fig. 1); and

a coil connected between the output terminal of the driver and the voltage battery output (28, 30, 26, 22, fig. 1; paragraph 0018, lines 1-11);

Claim Rejections - 35 USC § 103

- 12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 13. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. (US Pun No. 2004/0160725 A1 and Gu hereinafter) in view of Bird et al. (US Patent No. 4,929,884 and Bird hereinafter).

Gu discloses a driver circuit comprising:

a battery terminal and a ground terminal for connection to a voltage battery output and a ground battery output, respectively (24, GND, Fig.1);

an output terminal for driving a coil [claim 1] (fig. 1; paragraph 0018, lines 1-11) an energise FET having a source, a gate and a drain [claim 1] (30, fig.1)

a control FET having a source, a gate and a drain [claim 1] (28, fig.1)

a freewheel FET having a source, a gate and a drain [claim 1] (42, i.e., freewheel diode, fig. 1). Note that use of a freewheel FET in place of a freewheel diode will be covered below by Bird.

Gu did not expressly disclose:

where the energise FET is connected with source and drain between the output terminal and the ground terminal, and the control FET and freewheel FET are connected in series between the battery terminal and the output terminal, the sources and drains of the control and freewheel FETs being arranged reversely so that current flowing through the control and freewheel FETs in series flows from source to drain in one of the control and freewheel FETs and from drain to source in the other [claim 1];

a driver where the source of the energise FET is connected to the ground terminal and the drain is connected to the output terminal; the drain of the control FET is connected in common with the drain of the energise FET to the output terminal; and the drain of the freewheel FET is connected to the battery terminal and the source is connected to the source of the control FET [claim 2];

Nonetheless, these features are well known in the art and would have been an obvious modification of the driver circuit disclosed by Gu, as evidenced by Bird.

Bird discloses a high voltage semiconductor with integrated low voltage circuitry having:

where the energise FET is connected with source and drain between the output

Page 8

terminal and the ground terminal [claim 1] (53, fig. 3A; col. 9, lines 21-23), and the control FET and freewheel FET are connected in series between the battery terminal and the output terminal, the sources and drains of the control and freewheel FETs being arranged reversely so that current flowing through the control and freewheel FETs in series flows from source to drain in one of the control and freewheel FETs and from drain to source in the other [claim 1] (58, 56, fig. 3A) to block current and to prevent short circuit of coil. Note that item 53 is representing the energise FET, item 58 is representing the control FET and item 56 is representing the freewheel FET. Items 56 and 58 are in series and reversely arranged;

a driver where the source of the energise FET is connected to the ground terminal and the drain is connected to the output terminal; the drain of the control FET is connected in common with the drain of the energise FET to the output terminal; and the drain of the freewheel FET is connected to the battery terminal and the source is connected to the source of the control FET [claim 2] (items 53, 56, 58, fig. 3A);

Given the teaching of Bird, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Gu by employing the well known or conventional feature of coupling the control and energise FETs reversely and in series and employing a freewheel FET in place of a freewheel diode, such as disclosed by Bird, in order to allow the driver to operate effectively in the three modes (energise, freewheel and ring-off).

14. Claims 3 and 9 are rejected under 35 U.S.C 103(a) as being unpatentable over Gu et al. (US Pub. No. 2004/0160725 A1 and Gu hereinafter) in view of Bird et al. (US Patent No. 4,929,884) as applied to claim 1 above, and further in view of Yamashita et al. (US Patent No. 5,767,562 and Yamashita hereinafter).

Although the driver circuit disclosed by Gu and Bird show substantial features of the claimed invention (discussed in the paragraph above), they fail to disclose:

a common semiconductor substrate, wherein the drains the control FET and the energise FET are formed in the common semiconductor substrate and the drain of the freewheel FET is isolated from the common semiconductor substrate [claim 3];

A driver where the freewheel FET is a discrete FET formed in a separate semiconductor substrate [claim 9];

Nonetheless, these features are well known in the art and would have been an obvious modification of driver circuit disclosed by Gu in view of Bird, as evidenced by Yamashita.

Yamashita discloses a dielectrically isolated power IC having:

a common semiconductor substrate, where the drains the control FET and the energise FET are formed in the common semiconductor substrate and the drain of the freewheel FET is isolated from the common semiconductor substrate [claim 3] (items 11, 14, fig. 4; col. 5, lines 25-34, lines 52-54; items 11A, 14A, fig. 6A; lines 5-6, lines 62-67; items 11E, 14D, 14E, fig. 6G; col.. 7, lines 20-21) to provide both switches in one substrate. Note that both items 14D AND 14E would represent the control and energise FETs and item 11E would represent the isolated freewheel FET;

a driver where the freewheel FET is a discrete FET formed in a separate semiconductor substrate [claim 9] (items 11, 14, fig. 4; col. 5, lines 25-34, lines 52-54; items 11A, 14A, fig. 6A; lines 5-6, lines 62-67; items 11E, 14D, 14E, fig. 6G; col.. 7, lines 20-21) to provide both switches in one substrate. Note that both items 14D AND 14E in fig. 6G would represent the control and energise FETS and item 11E would represent the isolated freewheel FET;

Given the teaching of Yamashita, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Gu in view of Bird by employing the well known or conventional feature of employing both energise and control FETs in a common substrate and a freewheel FET in an isolated region, such as disclosed by Yamashita, in order to provide high speed switching in monolithic power IC.

15. Claims 4, 5, 6, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu in view of Bird as applied to claim 1.

Gu further discloses:

a driver comprising control circuitry integrally formed in the common semiconductor substrate, the control circuitry having a high voltage power rail connected to the battery terminal and a low voltage power rail connected to the ground terminal for powering the control circuitry from the battery and ground terminals [claim 4] (26A, fig. 2; paragraph 0031, lines 1-4). Note that 26A is a smart highside driver;

a driver where the control circuitry includes high-side control circuitry integrated

in the common semiconductor substrate and connected to the gates of the control and freewheel FETs to control the FETs; and low-side control circuitry integrated in the common semiconductor substrate and connected to the gate of the energise FET to control the energise FET [claim 5] (26, 28, 30, 42, 46, fig. 1). Note that item 42 is a free diode and item 46 is a recirculation diode;

a driver where the control FET is arranged to have a higher gate capacitance than the freewheel FET, and the control circuitry is arranged to turn the control FET fully on in the energise mode and, on switching from the energise mode to the freewheel mode, to connect the gates of the freewheel FET and the control FET together [claim 6] (items 28, 46 or freewheel diode, fig. 1; fig. 3; paragraph 0023, lines 1-11; paragraph 0024, lines 6-14; paragraph 0025, lines 1-12);

a driver where the control circuitry further comprises temperature and voltage overload protection for protecting one or more of the energise FET, the control FET and the freewheel FET [claim 7] (paragraph 0009, lines 1-5; paragraph 0024, lines 1-3);

a driver where the control circuitry is arranged to switch the FETs between an energise mode in which the energise FET is on and the freewheel FET is off, a freewheel mode in which the energise FET is off and both the control and freewheel FETs are off and a ring-off mode in which the energise FET is off and the control FET is off [claim 8] (paragraph 0023, lines 1-11, addresses energise mode; paragraph 0025, lines 1-12, addresses freewheel mode; paragraph 0028, lines 1-9, addresses ring-off mode;

16. Claim 13 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Gu et

al. (US Pub. No. 2004/016072 A1 and Gu hereinafter) in view of North et al. (US Patent No. 6,005,763 and North hereinafter).

Although the driver circuit disclosed by Gu shows substantial features of the clamed invention (disclosed above), it fails to disclose:

where the coil is a solenoid actuator having a mechanical actuator by current in the coil [claim13]

Nonetheless, this feature is well known in the art and would have been an obvious modification of the circuit disclosed by Gu, as evidenced by North.

North discloses pulse-energy controllers and methods of operation thereof having:

where the coil is a solenoid actuator having a mechanical actuator by current in the coil [claim 13] (col. 3, lines 1-4) to provide a mechanical actuator to the coil control circuit;

Given the teaching of North, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Gu by employing the well known or conventional feature of providing a solenoid with a mechanical actuator, such as disclosed by North, in order to provide a very short rise time to a current level exceeding the steady state current through the actuator coil.

17. Claims 14 and 15 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Gu et al. (US Pub. No. 2004/016072 A1 and Gu hereinafter) in view of Bird et al. (US Patent No. 4,929,884 and Bird hereinafter).

Gu discloses a method of operation of a coil control circuit, comprising:

a coil control circuit having a coil, a battery having positive and negative outputs, and a driver, the driver having an output terminal connected through the coil to a first one of the battery outputs, an energise FET connected between the output terminal and the other one of the battery outputs [claim 14] (items 28, 30, 22, 26, 24 fig. 1, note that the output terminal is between item 22 and item 30);

switching to an energise mode in which the energise FET (item 30) is on and the freewheel FET (item 42 or freewheel diode) is off to energise the coil (item 22) [claim 14] (fig. 1; paragraph 0023, lines 1-11);

switching to a freewheel mode in which the energise FET (item 30) is off and both the control and freewheel FETs (items 28, 42) are on to retain the coil energized [claim 14] (fig. 1; paragraph 0025, lines 1-12); and

switching to a ring-off mode in which the energise FET (item 30) is off and the control FET (item 28) is off to de-energise the coil [claim14] (fig.1; paragraph 0025, lines 1-12);

switching the control FET fully on in the energise mode and, on switching to the freewheel mode from the energise mode, connecting the gates of the freewheel and control FETs together to share charge to switch on the freewheel FET [claim 15] (items 28, 30, 42, i.e., freewheel diode, fig.1 paragraph 0023, lines 1-11; paragraph 0025, lines 1-12; paragraph 0028, lines 1-9);

Gu did not expressly disclose:

control and freewheel FETs of the like conductivity type connected reversely in series between the output terminal and the first one of the battery output [claim 14];

Nonetheless, these features are well known in the art and would have been an obvious modification of the driver circuit disclosed by Gu, as evidenced by Bird.

Bird discloses a high voltage semiconductor with integrated low voltage circuitry having:

control and freewheel FETs of the like conductivity type connected reversely in series between the output terminal and the first one of the battery output [claim 14] (58, 56, fig. 3A) to block current and to prevent short circuit of coil. Note that item 53 is representing the energise FET, item 58 is representing the control FET and item 56 is representing the freewheel FET. Items 56 and 58 are in series and reversely arranged;

Given the teaching of Bird, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Gu by employing the well known or conventional feature of coupling the control and energise FETs reversely and in series, and employing a freewheel FET in place of a freewheel diode, such as disclosed by Bird, in order to allow the driver to operate effectively in the three modes (energise, freewheel and ring-off).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Sitton whose telephone number is (571) 270-

Art Unit: 4158

3828. The examiner can normally be reached on Monday through Friday 8:00 AM- 4:30

PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Walter Benson can be reached on (571) 272-2227. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jan. 22, 2008

/Nelson Sitton/

Examiner, Art Unit 4158

/Walter Benson/

Supervisory Patent Examiner, Art Unit 4158